



#4 / Amata
A For
PATENT
8/23/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent application of: **Perumal Ratnam**

Atty Docket No.: **ALSCP003/B-6074**

Application No.: **09/375,702**

Examiner: **Terrell W. Fears**

Filed: **August 16, 1999**

Group: **2824**

Title: **A New Erase Technique to Improve the
Source Leakage of Flash EPROM Cells
During Source Erase**

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Commissioner of Patents and Trademarks, Washington, DC 20231 on Aug 9, 2000.

Signed: _____

Joyce L. Ferreira

AMENDMENT A

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated June 2, 2000, a response to which is due on a reset date of September 28, 2000, it is respectfully submitted that the Examiner amend the above identified patent application as follows:

RECEIVED
AUG 21 2000
10 2600 / 11 ROOM

In the Claims:

1. (Amended Once) A method for erasing a semiconductor device comprising:
- applying a voltage pulse at the source of the semiconductor device; and
 - applying a multiple step voltage pulse of the opposite polarity, said multiple step voltage pulse having at least a first voltage pulse and a second voltage pulse, at the gate of the semiconductor device;
- wherein said second voltage pulse is greater in magnitude than said first voltage pulse.

ALSCP003/B-6074

09/375,702